Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A packet processor comprising:

a control unit having a data input;

at least one encryption processor;

a first authentication processor;

a second authentication processor;

a local data bus, independent of the data input to the control unit, coupling the control unit to each of the encryption and authentication processors; and

a second data bus from the encryption processor to each authentication processor, including a data bus from the first authentication processor to the second authentication processor

wherein the control unit is configured to control the at least one encryption processor and the first and second authentication processors such that a first set of data and a second set of data sent from the at least one encryption processor to the first authentication processor and the second authentication processor, respectively, are processed by the first authentication processor and the second authentication processor while the at least one encryption processor processes a third set of data, and

wherein the at least one encryption processor, the first authentication processor and the second authentication processor are coupled to the local data bus independent of each other and independent of the control unit.

2. (Previously Presented) A packet processor as recited in claim 1, wherein said data input of the control unit is coupled to a processor bus, and wherein each of said encryption and authentication processors comprises a data input coupled to the processor bus.

3. (Previously Presented) A packet processor as recited in claim 1, wherein said data input of the control unit is coupled to a processor bus and each of said encryption and authentication processors comprises a data input to the processor bus and means for reading and writing data on the processor bus.

4. (Previously Presented) A packet processor as recited in claim 1, wherein said second data bus comprises a daisy-chain connection between the encryption and authentication processors.

5. (Currently Amended) A method of processing data packets comprising:

coupling a control unit to a first data bus;

receiving first and second data packets in the control unit from the first data bus;

coupling a plurality of processors to a second data bus independent of each other and independent of the control unit;

providing ~~a~~ the plurality of processors in data communication with the control unit over ~~a~~ the second data bus, independent of the first data bus, said processors including at least one encryption processor and at least one authentication processor;

providing data of the first data packet from the control unit to said at least one encryption processor, over the second data bus;

processing said data from the first data packet with said at least one encryption processor to provide output data for the first data packet from said at least one encryption processor;

communicating said output data for the first data packet from said at least one encryption processor to said at least one authentication processor for further processing; and

providing data from the second data packet to said at least one encryption processor and processing the data from the second data packet in the at least one encryption processor while said at least one authentication processor further processes the output data for the first data packet.

6. (Cancelled)

7. (Previously Presented) A method as recited in claim 5, wherein said at least one authentication processor comprises a first and second authentication processors.

8. (Previously Presented) A method as recited in claim 5, wherein said step of communicating the output data comprises communicating said output data over a daisy-chain connection between said processors.

9. (Currently Amended) A method of processing data in a computer, the method comprising the steps of:

coupling an encryption processor and at least one authentication processor to a data bus independent of each other;

performing encryption on a first data packet within ~~an~~ the encryption processor; and

after completion of the encryption of the first data packet,

performing authentication of the first data packet within the at least one authentication processor connected to the encryption processor by ~~a~~ the data bus, and

performing encryption of a second data packet within the encryption processor prior to completion of authentication of the first data packet.

10. (Original) The method of claim 9, wherein the authentication is a first authentication, further comprising the step of performing a second authentication on the first data packet of data.

11. (Original) The method of claim 10, wherein the first authentication is performed on the encrypted first data packet.

12. (Original) The method of claim 10, wherein the first authentication appends data to the encrypted first data packet.

13. (Original) The method of claim 12, wherein the second authentication is performed on the encrypted first data packet and the appended data.

14. (Original) The method of claim 10, further comprising the step of performing the encryption of the second data packet after beginning the second authentication of the first data packet.

15. (Currently Amended) A method of processing data, the method comprising the steps of:

coupling an encryption processing module and a first authentication processing module to a data bus independent of each other;

encrypting a first data packet with ~~an~~ the encryption processing module;

authenticating the encrypted first data packet with ~~a~~ the first authentication processing module;

encrypting a second data packet with the encryption processing module while authenticating the first data packet with the first authentication processing module connected to the encryption processing module by ~~a~~ the data bus; and

authenticating the second data packet with the first authentication processing module.

16. (Currently Amended) ~~A system~~An apparatus for processing data, comprising:

a computer having a data storage device connected thereto, wherein the data storage device stores data;

one or more computer programs, performed by the computer, for performing encryption on a first data packet within an encryption processor, and, after completion of the encryption of the first data packet, performing authentication of the first data packet in at least one

authentication processor connected to the encryption processor by a data bus, and performing encryption of a second data packet within the encryption processor prior to completion of authentication of the first data packet,

wherein the encryption processor and the at least one authentication processor are coupled to the local data bus independent of each other.

17. (Original) The apparatus of claim 16, wherein the authentication is a first authentication, further comprising means for performing a second authentication on the first data packet of data.

18. (Original) The apparatus of claim 17, wherein the first authentication is performed on the encrypted first data packet.

19. (Original) The apparatus of claim 17, wherein the first authentication appends data to the encrypted first data packet.

20. (Original) The apparatus of claim 19, wherein the second authentication is performed on the encrypted first data packet and the appended data.

21. (Original) The apparatus of claim 17, further comprising the means for performing the encryption of the second data packet after beginning the second authentication of the first data packet.

22. (Cancelled)

23. (Currently Amended) An article of manufacture comprising a computer program carrier readable by a computer and embodying one or more instructions executable by the computer to perform method steps for processing data, the method comprising the steps of:

performing encryption on a first data packet with an encryption processor; and

after completion of the encryption of the first data packet,

performing authentication of the first data packet in at least one authentication processor connected to the encryption processor by a data bus, and

performing encryption of a second data packet within the encryption processor prior to completion of authentication of the first data packet,

wherein the encryption processor and the at least one authentication processor are coupled to the data bus independent of each other.

24. (Original) The article of manufacture of claim 23, wherein the authentication is a first authentication, further comprising the step of performing a second authentication on the first data packet of data.

25. (Original) The article of manufacture of claim 24, wherein the first authentication is performed on the encrypted first data packet.

26. (Original) The article of manufacture of claim 24, wherein the first authentication appends data to the encrypted first data packet.

27. (Original) The article of manufacture of claim 26, wherein the second authentication is performed on the encrypted first data packet and the appended data.

28. (Original) The article of manufacture of claim 24, further comprising the step of performing the encryption of the second data packet after beginning the second authentication of the first data packet.

29. (Currently Amended) An article of manufacture comprising a computer program carrier readable by a computer and embodying one or more instructions executable by the computer to perform method steps for processing data, the method comprising the steps of:

encrypting a first data packet with an encryption processor;

authenticating the encrypted first data packet with a first authentication processor connected to the encryption processor by a data bus;

encrypting a second data packet with the encryption processor while authenticating the first data packet with the first authentication processor; and

authenticating the second data packet with the first authentication processor,

wherein the encryption processor and the first authentication processor are coupled to the data bus independent of each other.

30. (Currently Amended) A method of processing data packets comprising:

coupling a control unit to a first data bus;

coupling a plurality of processors to a second data bus independent of each other and independent of the control unit;

receiving a first data packet in the control unit from the first data bus;

providing ~~a~~ the plurality of processors in data communication with the control unit over ~~a~~ the second data bus, independent of the first data bus, said processors including at least one encryption processor and at least one authentication processor;

providing data of the first data packet from the control unit to multiple processors, over the second data bus;

processing said data from the first data packet with said multiple processors in parallel.

31. (Previously Presented) A method as recited in claim 30, wherein said plurality of processors comprises at least one encryption processor and a plurality of authentication processors.

32. (Previously Presented) A method as recited in claim 5, wherein said at least one authentication processor performs an integrity check of said output data.

33. (Previously Presented) A method as recited in claim 32, wherein said at least one authentication processor comprises an HMAC core.

34. (Previously Presented) A method as recited in claim 32, wherein said integrity check is performed using HMAC- key hashing.

35. (Currently Amended) A method of processing data packets comprising:

coupling a control unit to a first data bus;

receiving first and second data packets in the control unit from the first data bus;

providing a plurality of processors in data communication with the control unit over a first local data bus, independent of the first data bus, the plurality of processors being coupled to the first local data bus independent of each other and independent of the control unit, said processors including at least one encryption processor and at least one authentication processor, the at least one authentication processor being coupled to the at least one encryption processor by a second local data bus separate from the first data bus and the first local data bus;

providing data of the first data packet from the control unit to said at least one encryption processor, over the first local data bus;

processing said data from the first data packet with said at least one encryption processor to provide output data for the first data packet from said at least one encryption processor;

communicating said output data for the first data packet from said at least one encryption processor to said at least one authentication processor via the second local data bus for further processing; and

providing data from the second data packet to said at least one encryption processor for processing by the at least one encryption processor , while said at least one authentication processor further processes the output data for the first data packet.

36. – 42. (Cancelled)

43. (Currently Amended) A packet processor apparatus for connection to a computer through a processor bus, the packet processor system comprising:

a controller having means for connection to the processor bus for communicating data of data packets to or from the processor bus;

a plurality of hardware processor devices, each capable of processing data simultaneous with the processing of data by at least one other of said hardware processor devices;

a local bus connecting the controller to the plurality of processor devices for communication of instructions from the controller to each hardware processor, wherein said instructions include instructions for processing data from a first packet in a first one of the plurality of hardware processor devices and processing output from the first hardware processor device with a second one of the hardware processor devices, while data from a second packet is processed by the first hardware processor device,

wherein the plurality of hardware processor devices are coupled to the local bus independent of each other and independent of the controller.

44. (Previously Presented) A packet processor apparatus as recited in claim 43, wherein the plurality of hardware processor devices comprise at least one encryption processor and at least one authentication processor.

45. (Previously Presented) A packet processor apparatus as recited in claim 43, wherein the first hardware processor device comprises an encryption processor device and wherein the second hardware processor device comprises an authentication processor device.

46. (Currently Amended) A packet processor apparatus for connection to a computer that operates on data from data packets communicated over a processor bus, wherein

cryptographic and authentication functions are performed on the data packets prior to or after operation on the packet data by the computer, the packet processor comprising:

a controller having means for connection to the processor bus for communicating data of data packets to or from the processor bus;

at least one encryption processor devices;

at least one authentication processor device;

a local bus connecting the controller to the encryption processor device and the authentication processor devices for communication of control instructions; and

wherein said controller is configured to provide control instructions for processing data from a first packet in the at least one encryption processor devices and processing output from the at least one encryption processor device with the at least one authentication processor device, while data from a second packet is processed by the at least one encryption processor device, and

wherein the at least one encryption processor device and the at least one authentication processor device are coupled to the local bus independent of each other and independent of the controller.

47. (New) A packet processor as recited in claim 1, wherein the at least one encryption processor, the first authentication processor and the second authentication processor are configured to control the local data bus independently of the control unit.

48. (New) A packet processor as recited in claim 1, wherein only the encryption processor is active.

49. (New) A packet processor as recited in claim 1, wherein only the encryption processor and the first authentication processor are active.